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Design & Simulation Of 3-Phase, 15-Level Inverter with Reverse Voltage Topology

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Abstract:
Multilevel inverters have been widely accepted for high-power high-voltage applications. Their performance is highly superior to that of conventional Seven-level inverters due to reduced harmonic distortion, lower electromagnetic interference, and higher dc link voltages. In this paper, a new topology with a reversing-voltage component is proposed to improve the multilevel performance. This topology requires fewer components compared to existing inverters (particularly in higher levels) and requires fewer carrier signals and gate drives. Therefore, thecomplexity is greatly reduced particularly for higher output voltage levels. The Proposed 15-level inverter is modelled and simulated in Matlab 2012a using Simulink and Sim Power Systems set tool boxes
Keywords*:* Multilevel inverter, power electronics, SPWM, topology.

I. INTRODUCTION

Advancement in the research of Power electronic invertersis still increasing with the rapid demands in electrical systems. The emergence of multilevel inverters has been in increase since the last decade. These new types of converters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum[10].

Multilevel converters are mainly utilized to synthesis a desired single- or three-phase voltage waveform. Thedesired multi-staircase output voltage is obtained by combining several dc voltage sources. Solar cells, fuel cells,batteries and ultra-capacitors are the most common independent sources used [1]. One important application ofmultilevel converters is focused on medium and high-power conversion. Nowadays, there exist three commercialtopologies of multilevel voltage-source inverters: neutral point clamped (NPC), cascaded H-bridge (CHB), and flyingcapacitors (FCs)[2]. Among these inverter topologies, cascaded multilevel inverter reaches the higher output voltage and power levels (13.8 kV,30 MVA) and the higher reliability due to its modular topology[3].

Diode-clamped multilevel converters are used in conventional high-power ac motor drive applications likeconveyors, pumps, fans, and mills. They are also utilized in oil, gas, metals, power, mining, water, marine, andchemical industries. They have also been reported to be used in a back-to-back configuration for regenerativeapplications[4]. Flying capacitor multilevel converters have been used in high-bandwidth high-switching frequencyapplications such as medium-voltage traction drives. Finally, cascaded H-bridge multilevel converters have beenapplied where high power and power quality are essential, for example, static synchronous compensators active filterand reactive power compensation applications, photovoltaic power conversion, uninterruptible power supplies, andmagnetic resonance imaging. Furthermore, one of the growing applications for multilevel motor drives is electric andhybrid power trains.

For increasing voltage levels the number of switches also will increase in number. Hence the voltage stresses andswitching losses will increase and the circuit will become complex. By using the proposed topology number ofswitches will reduce significantly and hence the efficiency will improve.

A multi-stage inverter using three-state converters is being analyzed for multipurpose applications, such asactive power filters, static var compensators and machine drives for sinusoidal and trapezoidal currentapplications. The great advantage of this kind of converter is the minimum harmonic distortion obtained.

The circuit of Fig.1 shows the basic topology of oneconverter used for the implementation of multi-stageconverters.It is based on the simple, four switches converter,used for single phase inverters or for dual converters. Theseconverters are able to produce three levels of voltage in theload: +Vdc, -Vdc, and Zero[7].

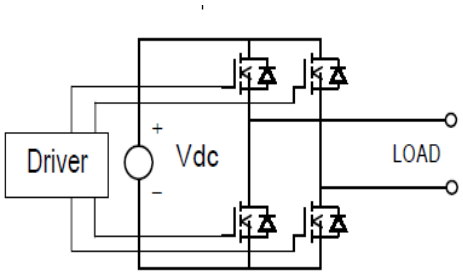

Fig.1. Basic idea diagram of three-level module for building multi stage inverter

This paper mainly focuses on the general multilevel inverter schematic. A general method of multilevel modulation phase disposition (PD) SPWM is utilized to drive the inverter and can be extended to any number of voltage levels. Here , in this paper the proposed multilevel scheme extended up to 15-levels.. In this work, the asymmetric 15 level inverter is presented. This inverter is designed to avoid the regeneration problem - power flow from the load to the inverter - in some of the power cells. This is achieved by obtaining the firing angles associated with the power cells considering a minimum load voltage THD. The simulation and experimental results of the proposed 15-level inverter topology are also presented. Finally, a power flow analysis is accomplished and simulated results show the feasibility of this approach

II. PROPOSED 15-LEVEL INVERTER

Multilevel inverters are the alternative for medium voltage applications. Within the inverters types there are symmetric and asymmetric topologies. The asymmetric inverters have different DC voltage values. The most common topology is when the different cells are implemented in cascade arrangement, where the DC voltage are in multiples of 3, obtaining an AC voltage with $3^n = 27$ levels (n = 3 cascaded inverters). This topology provides a load voltage with low harmonic content, THD <; 3%. However, this high quality voltage has a non-negligible drawback, which is the presence of regeneration in some of the inverters, independent of load type[1]. This phenomenon is due to the modulation technique (Nearest Level Modulation) used by this inverter. In this work, the asymmetric 15 level inverter is presented. This inverter is designed to avoid the regeneration problem - power flow from the load to the inverter - in some of the power cells. This is achieved by obtaining the firing angles associated with the power cells considering a minimum load voltage THD. Finally, a power flow analysis is accomplished and simulated results show the feasibility of this approach.

Fig.2 shows the proposed inverter fed to 3-phase a.c load and Fig.3 shows the simplified diagram with three inverters per phase.

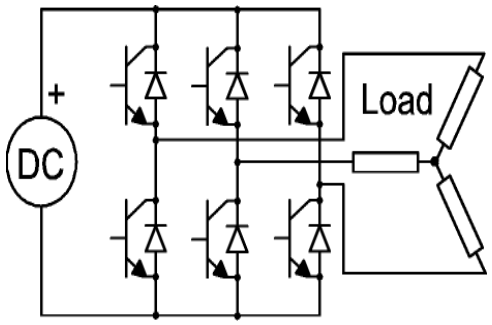

Fig.2. Basic idea diagram of three-phase inverter

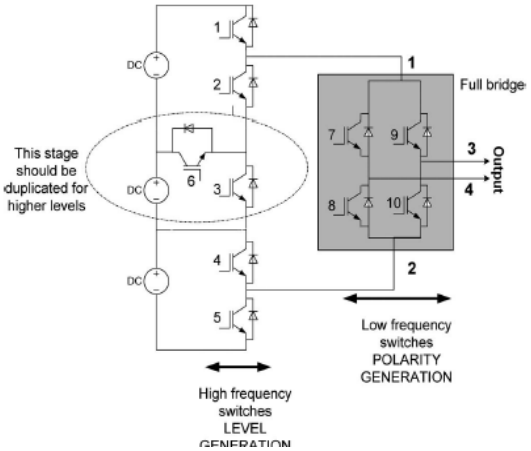

Fig.3. Schematic of seven level inverter in single phase

The most commonly used multilevel topologyis the diode clamped inverter, in which the diode isused as the clamping device to clamp the dc busvoltage so as to achieve steps in the output voltage.

A three-level diode clamped inverter consistsof two pairs of switches and two diodes. Each switchpairs works in complimentary mode and the diodesused to provide access to mid-point voltage. In athree-level inverter each of the three phases of theinverter shares a common dc bus, which has beensubdivided by two capacitors into three levels. TheDC bus voltage is split into three voltage levels byusing two series connections of DC capacitors,C1 andC2. The voltage stress across each switching device islimited to Vdc through the clamping diodes Dc1 andDc2. It is assumed that the total dc link voltage is Vdcand mid point is regulated at half of the dc linkvoltage, the voltage across each capacitor is Vdc/2(Vc1=Vc2=Vdc/2).[1]

A. Switching Sequences:

In order to avoid unwanted voltage levels during switchingcycles, the switching modes should be selected so that theswitching transitions become minimal during each mode transfer.This will also help to decrease switching power dissipation.

In order to produce 15- levels by Sinusoidal Pulse Width Modulation (SPWM), three saw-toothwaveforms for carrier and a sinusoidal reference signal formodulator are required as shown in Fig. 4.

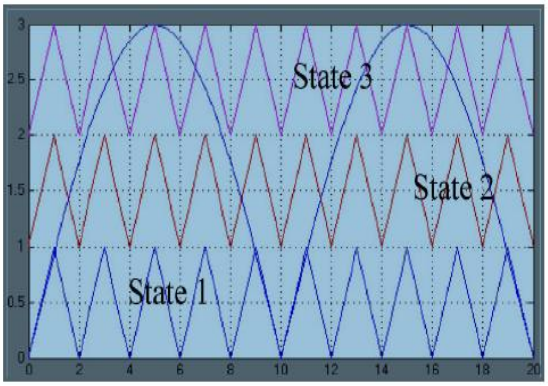

Fig. 4.SPWM carrier and modulator for proposed 15-level inverter

III. MATLAB BASED SIMULATION& RESULTS

A. MATLAB based simulation :

Fig.4. shows the complete MATLAB based simulation masked diagram of the proposed 15-level, 3-phase inverter.

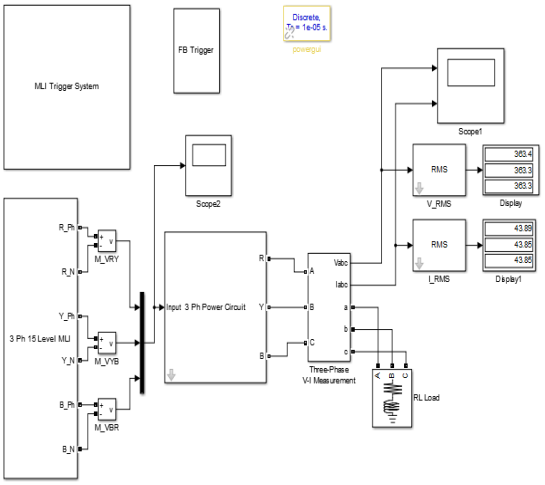

Fig.4.MATLAB based simulation masked diagram of the proposed 15-level, 3-phase inverter

Fig.5. shows the input DC voltage source to the proposed 15-level, 3-phase inverter

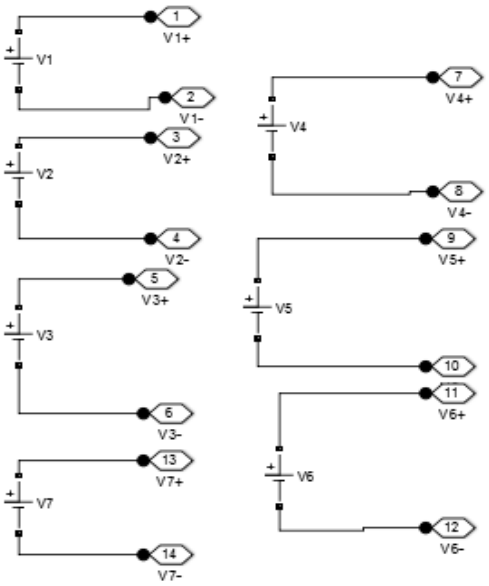

Fig.5. Input DC voltage source to the proposed 15-level, 3-phase inverter

Fig.6. shows power electronic based bridge circuit of the proposed 15-level, 3-phase inverter

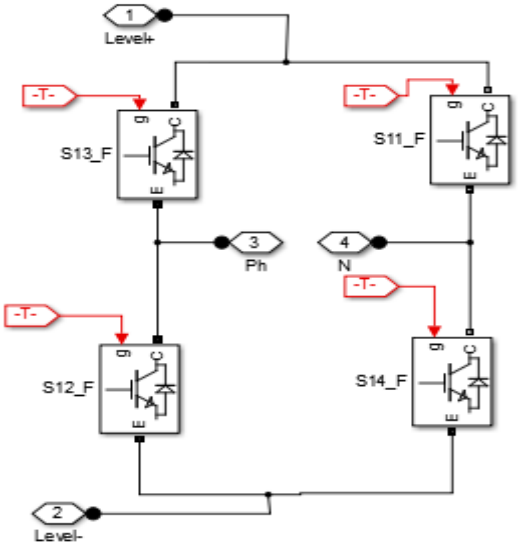

Fig.6. Simulation diagram of power electronic based bridge circuit of the proposed 15-level, 3-phase inverter

Fig.7. shows the gate controlled pulse to the proposed 15-level, 3-phase inverter

Fig.8.shows the inversion of DC to 3-phase MATLAB based simulation diagram.

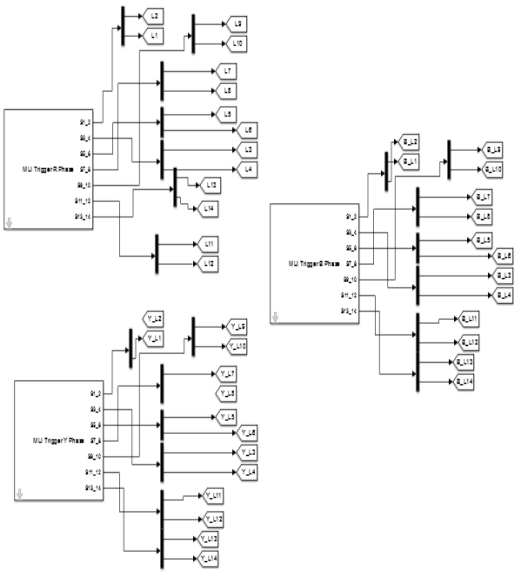

Fig.7. Gate controlled pulse to the proposed 15-level, 3-phase inverter

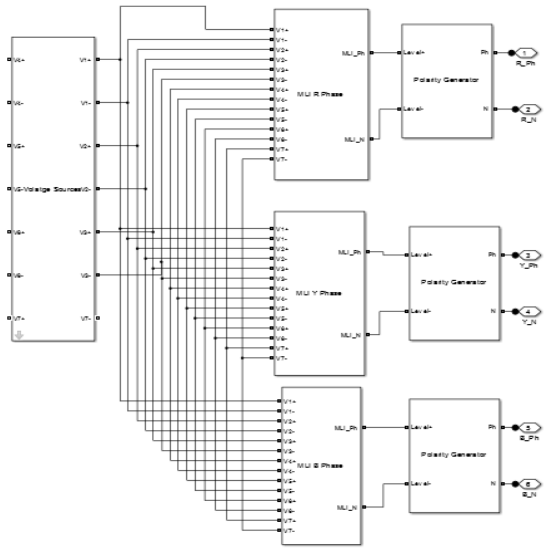

Fig.8. DC to AC 3-phase inversion MATLAB based simulation diagram.

Simulation parameters for the proposed 15-level, 3-phase inverter is given by in the Table.1

***B. Simulation Results*:**

Fig.9. shows the 3-phase, 15-level output voltage waveform from the proposed inverter.

Fig.10. shows the THD calculation of proposed 3-phase, 15-level inverter using powergui FFT Analysis tool.

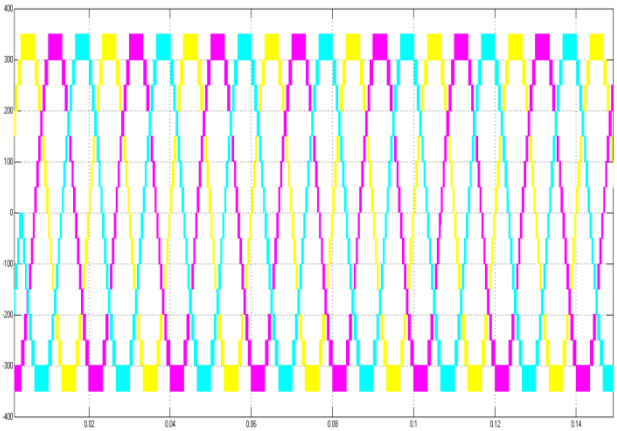

Fig.9. 3-Phase, 15-level output voltage waveform from the proposed inverter

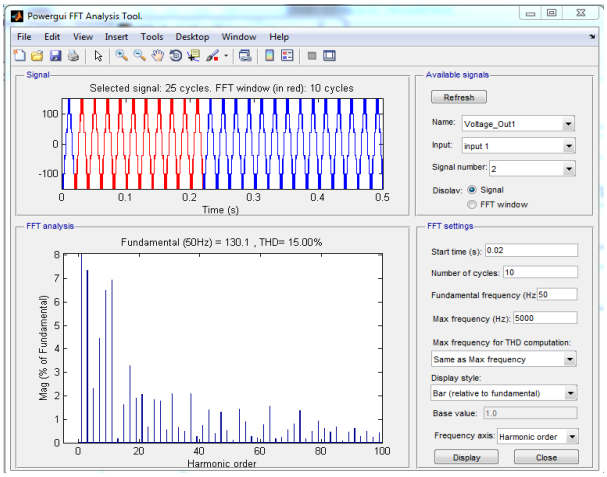

Fig.10. THD calculation of proposed 3-phase, 15-level inverter using powergui FFT Analysis tool

Fig.11. shows the 3-phase voltage and 3-phase current waveform from the proposed inverter.

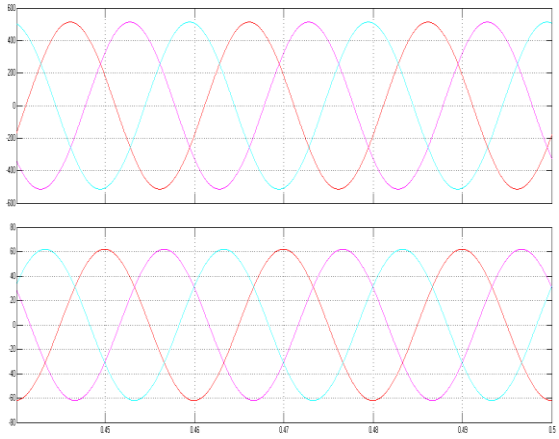

Fig.11. 3-phase voltage (upper) and 3-phase current (lower) waveform from the proposed inverter respectively

Table .2. Shows the r.m.s values from phase voltages and currents

TABLE1.SIMULATION SPECIFICATIONS

Parameter	*Rating*
Input DC supply (V)	50V
IGBT/Diode Internal Resistance Ron	1 m Ω
Snubber Resistance , Rs (Ω)	1μΩ
Nominal frequency (Hz)	50 Hz
Active Power (W)	10KW
Reactive Power (Var)	8Kvar
Damping factor of filter	0.8

TABLE.2. RMS VALUES OF OUTPUT RESPONSES OF PROPOSED INVERTER

Output Response	*RMS Value*
Phase A voltage (V)	363.4
Phase B voltage (V)	363.3
Phase C voltage (V)	363.3
Phase A Current (A)	43.89
Phase B Current (A)	43.85
Phase C Current (A)	43.85

IV. CONCLUSION

An efficient 3-phase, 15-level inverter is presented in the paper. The resultant simulation graphs show the accuracy of the proposed inverter.High performance switchesare adopted to reduce the conductionlosses and improve the efficiency.Experimental results that confirm the feasibilityof the proposed 3-phase, 15-level inverter.Finally, MATLAB based simulink results showns the THD value at reasonable level.

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